7th International Workshop on Parallel Matrix Algorithms and Applications

7th International Workshop on Parallel Matrix Algorithms and Applications (PMAA 2012) 28-30 June 2012, Birkbeck University of London, UK

- Website: http://www.dcs.bbk.ac.uk/pmaa2012/
- Responsible partner: IICT-BAS

Technical digest:

The topics of this workshop are relevant to the HP-SEE project and the technology watch not only because it was a forum for an exchange of ideas, insights and experiences in different areas of parallel computing (Multicore, Manycores and GPU) but also because of the well presented stream devoted to Energy aware performance metrics.

Recent years have seen a dramatic change in core technology. Voltage and thus frequency scaling has stopped. Thus, to continue the exponential overall improvements technologies have turned into multi-core chips and parallelism at all scales. With these new trends, a series of new problems arise: how to program such complex machines and how to keep pace with the very fast increase in power requirements. In his invited presentations Dr. Becas (IBM) concentrated on the latter, and the focal point of his recent research was the energy aware performance metrics. It was demonstrated that traditional energy aware performance metrics that are directly derived from the old Flop/sec performance metric have serious shortcomings and can potentially give a completely different picture reality. Instead, it was shown that by optimizing functions of time to solution and energy at the sae time, one can get a much more clear picture. This immediately implies a change in the way we gauge performance of computing systems: we need to abandon the single benchmark, and rather opt for a set of benchmarks, that ae basic kernels with widely different characteristics.